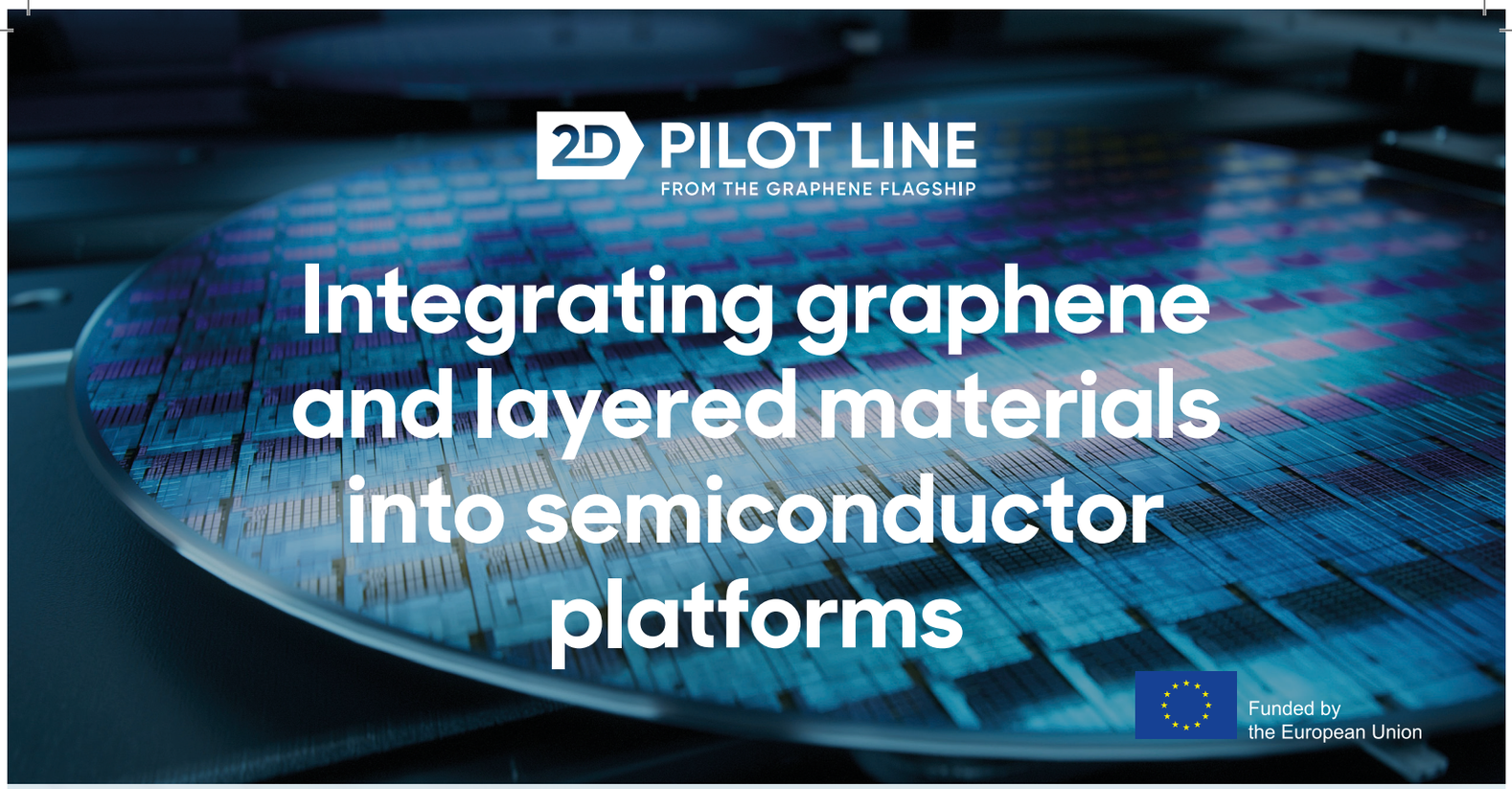

Discover the 2D-EPL

Born within the innovative ecosystem pioneered by the EU-funded Graphene Flagship project, the new 2D Experimental Pilot Line (2D-EPL) will be the first graphene foundry to integrate graphene and layered materials into semiconductor platforms.

The €20M project integrates several Graphene Flagship members to pioneer the fabrication of new prototype electronics, photonic devices and sensors integrating graphene and layered materials. The 2D-EPL will offer comprehensive prototyping services to companies, research centres and academics laying the groundwork for the integration of graphene and layered materials on established semiconductor platforms that use silicon technologies.

2D-EPL services

The project will offer two different kinds of integration services:

- Five Multi-Purpose Wafer (MPW) runs with a specific application scope will be organized by the 2D-EPL. In these MPW runs, the processing scheme will be defined through process design kits and the customer will be able to share the cost of the processing.
- The pilot line sites, AMO, imec and VTT, are also open to tailor-designed 2D integrations for specific customer applications which can benefit from the progress and lessons learned throughout the project.

Meet our partners

The 2D Experimental Pilot Line gathers key European players covering the whole value chain, including tool manufacturers, chemical and material providers and semiconductor fabrication lines.

CHALMERS UNIVERSITY OF TECHNOLOGY · AIXTRON · imec · AMO · VTT · SÜSS MicroTec · Graphenea · micro resist technology · ihp solutions · OXFORD INSTRUMENTS

Important Run 3 Dates

1 April 2023: Call opens for applications, design rules and PDK available
18 June 2023: Call closes, design freeze
1 October – 30 November 2023: MPW run

2D-EPL MPW run 3

The third MPW run is mainly intended towards electronics but can also include sensor devices (e.g. Hall sensor, but via opening on graphene is not in the scope of this run) and will be provided by AMO GmbH. The design of the device can be adjusted within the specifications. The offered device structure is a GFET (Fig. 1) consisting of the following fabrication steps:

- Back gate
- Dielectric deposition & vias opening
- Fabrication of adhesion pads
- Wafer scale graphene transfer & patterning
- Top contacts fabrication
- Encapsulation & vias opening (not on top of graphene)

The summary of the key parameters for a device with local back gate is shown in the table below.

Summary

Parameter		Value
Graphene Mobility		>1000 cm²/Vs
Avg. Sheet Resistance	n=5x1012 cm-2: CNP:	~1 kΩ ~4 kΩ
Avg. Contact Resistance	n=5x1012 cm-2: CNP:	~1 kΩ µm ~4 kΩ µm
Minimum working devices		>80 %
Dirac point		<15 V
Safe gate-source voltage range		± 20 V

Timeline

Application Phase	1 Apr – 18 Jun
Final Layout Submission and PO	25 Jun
MPW Run 3	1 Oct – 30 Nov
Delivery	1 Dec – 21 Jan 2024

- During the application phase, interested clients can contact us via the contact form and receive further information about the run in a first meeting.
- Final Layout Submission and PO must be received by 25 June.
- The chips are expected to be delivered in December 2023.

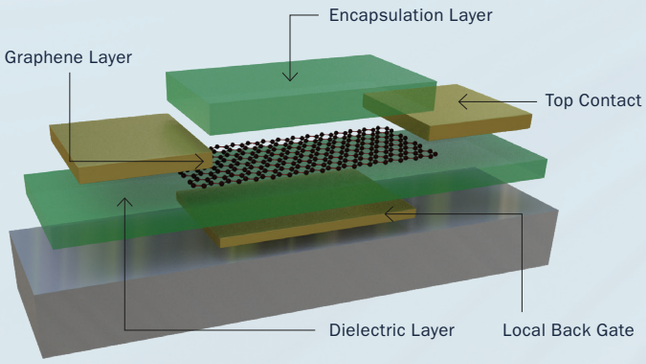

Figure 1: Scheme with the different layers of the final GFET structure.

Specifications

Substrate
- Material: Silicon
- Basic die size: 1x1 cm²

Resolution
- General design rule: 10 µm for in-layer critical dimension and over-layer alignment

Characterization
- Raman characterization
- Electrical measurement for as-fabricated reference devices
- General optical inspection of your devices

Costs
- 1 300,-€ set price for four dies with identical design (1x1 cm²)
- Each die more with identical design costs 250,-€ in addition

Layer Thicknesses		Value
Rigid Substrate	Si/SiO_2	90 nm
Back Gate Contact	Ti/Pd	5nm/40nm
Dielectric Layer	Al_2O_3	40 nm
Adhesion Layer for Top Contact Pad	Ni	25 nm
Graphene	Single layer, CVD on Cu	
Top Contact	Pd	40 nm
Encapsulation	Al_2O_3	80 nm

About AMO

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